CLAIMS

What is claimed is:

1. A method providing a semiconductor device, the semiconductor including a first layer desired to be etched, the method comprising the steps of:

(a) providing an antireflective coating (ARC) layer having antireflective properties;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching the first layer, a first portion of the first layer and a second portion of the ARC layer being exposed by the pattern;

(c) etching the first portion of the first layer and the second portion of the ARC layer; and

(d) removing the resist layer utilizing a plasma etch, the ARC layer being resistant to the plasma etch.

2. The method of claim 1 wherein the ARC layer providing step (a) further includes the steps of:

(a1) depositing the ARC layer.

3. The method of claim 1 wherein the ARC layer further includes an SiON layer and wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas.

4. The method of claim 3 wherein the plasma further includes four percent of the forming gas.

5. The method of claim 3 further comprising the step of:

(e) providing a wet preclean after the plasma etching step (d).

6. The method of claim 1 wherein the ARC layer is a SiON ARC layer and wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

7. A semiconductor device comprising:

a plurality of memory cells including a plurality of stacked gates; and

wherein the plurality of stacked gates are provided using an antireflective coating (ARC) layer that is resistant to removal by a plasma etch, a portion of the semiconductor device is provided using a resist layer, the resist layer being removed using the plasma etch.

8. The semiconductor device of claim 7 wherein the ARC layer further includes an SiON layer and wherein the resist layer is removed using by the plasma etch which uses a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas.

9. The semiconductor device of claim 8 wherein the plasma further includes four percent of the forming gas.

10. The semiconductor device of claim 7 wherein the ARC layer is a SiON ARC layer and wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

11. The semiconductor device of claim 7 further comprising:

a plurality of logic cells;

wherein the plurality of logic cells are defined using the ARC layer that is resistant to removal by the plasma etch.

12. The semiconductor device of claim 11 wherein a portion of the semiconductor device provided using the resist layer includes the plurality of memory cells.